IN THE CLAIMS:

No claims have been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (previously presented) A metallization structure for a semiconductor device, comprising:

a substrate comprising a substantially planar upper surface; and

a conductive line for transmitting a signal laterally across the substrate, the conductive line consisting essentially of:

a metal layer defining a pattern on a portion of the substrate upper surface;

a single conducting layer overlying and substantially coextensive with the metal layer, the metal layer and the single conducting layer having substantially aligned sidewalls and the single conducting layer defining an upper surface of the conductive line; and

metal spacers flanking and extending at least substantially to a height of the sidewalls of the single conducting layer and metal layer.

2. (original) The metallization structure of claim 1, further comprising a dielectric layer on the substrate upper surface and underlying the metal layer.

3. (original) The metallization structure of claim 2, wherein the dielectric layer is silicon oxide or BPSG.

4. (original) The metallization structure of claim 1, wherein the metal layer is a first metal layer comprising Ti, Ta, W, Co or Mo or alloys or compounds thereof, including TaN or TiN.

5. (original) The metallization structure of claim 4, further including a second metal layer disposed between the first metal layer and the substrate and comprising TiN, TiW, WN, or TaN.

6. (original) The metallization structure of claim 5, wherein the first metal layer comprises titanium or titanium nitride.

7. (original) The metallization structure of claim 1, wherein the metal layer is titanium or titanium nitride.

8. (previously presented) The metallization structure of claim 1, wherein the single conducting layer is selected from the group comprising aluminum and copper.

9. (previously presented) The metallization structure of claim 8, wherein the single conducting layer is an aluminum-copper alloy.

10. (original) The metallization structure of claim 1, wherein the metal spacers comprise at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN.

11. (previously presented) The metallization structure of claim 1, wherein the metal spacers are titanium or titanium nitride.

12. (previously presented) The metallization structure of claim 1, further comprising a dielectric layer on the single conducting layer and having sidewalls aligned with the sidewalls of the single conducting layer, the metal spacers extending along the sidewalls of the dielectric layer.

13. (original) The metallization structure of claim 12, wherein the dielectric layer comprises a low dielectric constant material.

14. (original) The metallization structure of claim 13, wherein the dielectric layer is fluorine-doped silicon oxide.

15. (original) The metallization structure of claim 1, wherein the metal layer and the metal spacers comprise the same metal.

16. (previously presented) A metallization structure for a semiconductor device, comprising:

a substrate having a metal layer extending over the substrate, the metal layer at least underlying a conductive line, the conductive line for transmitting a signal across the substrate;

a dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer, the at least one sidewall of the aperture defining the conductive line;

a metal spacer abutting at least one sidewall of the at least one sidewall of the aperture and in contact with the dielectric layer, the metal spacer in contact with the underlying metal layer; and

a conductive layer in contact with the metal layer and the metal spacer, the metal spacer and the conductive layer substantially filling the aperture, the conductive layer having an upper surface substantially coincident with an upper surface of the dielectric layer.

17. (original) The metallization structure of claim 16, wherein the metal layer comprises tantalum, titanium, tungsten, cobalt, molybdenum, or an alloy or a compound of any thereof, including TaN and TiN.

18. (original) The metallization structure of claim 17, wherein the metal layer is titanium or titanium nitride.

19. (previously presented) The metallization structure of claim 16, wherein the metal spacer includes at least one layer of metal comprising tantalum, titanium, tungsten, cobalt, molybdenum, or alloys or compounds thereof, including TaN and TiN.

20. (previously presented) The metallization structure of claim 19, wherein the metal spacer is titanium or titanium nitride.

21. (original) The metallization structure of claim 16, wherein the substrate comprises a dielectric layer underlying the metal layer.

22. (original) The metallization structure of claim 21, wherein the dielectric layer underlying the metal layer is silicon oxide or BPSG.

23. (previously presented) The metallization structure of claim 16, wherein the metal layer and the metal spacer comprise the same metal.

24. (original) The metallization structure of claim 16, wherein the metal layer is a first metal layer comprising Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

25. (original) The metallization structure of claim 24, further including a second metal layer disposed between the first metal layer and the substrate and comprising TiN, TiW, WN, or TaN.

26. (previously presented) A metallization structure for a semiconductor device, comprising:

a substrate having a metal layer extending over the substrate, the metal layer at least underlying a conductive line, the conductive line for transmitting a signal across the substrate;

a dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer, the at least one sidewall of the aperture defining the conductive line;

a metal spacer abutting at least one sidewall of the at least one sidewall of the aperture and in contact with the dielectric layer, the metal spacer in contact with the underlying metal layer;

a conductive layer in contact with the metal layer and the metal spacer, the metal spacer and the

conductive layer nearly filling the aperture; and

at least one upper metal layer on the conductive layer comprising Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN, the at least one upper metal layer being disposed within the aperture laterally adjacent the metal spacer and having an upper surface substantially coincident with an upper surface of the dielectric layer and an uppermost extent of the metal spacer.

27. (original) The metallization structure of claim 26, wherein the at least one upper metal layer comprises a plurality of upper metal layers.

28. (previously presented) The metallization structure of claim 26, wherein the at least one upper metal layer comprises titanium or titanium nitride.

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100. (previously presented) The metallization structure of claim 2, wherein the dielectric layer extends completely underneath the conductive line.

101. (previously presented) The metallization structure of claim 16, wherein the aperture contains conductive material.

102. (previously presented) A structure for transmitting a signal across a semiconductor device, the structure comprising:

a substrate comprising a substantially planar upper surface; and

a conductive line extending over the upper surface and isolated therefrom by a dielectric layer at least underlying the conductive line, the conductive line consisting essentially of:

a metal layer above the dielectric layer, the metal layer defining a pattern on a portion of the substrate upper surface;

a single conducting layer overlying and substantially coextensive with the metal layer, the metal layer and the single conducting layer having substantially aligned sidewalls,

wherein an upper surface of the single conductive layer defines an upper surface of the conductive line; and

metal spacers flanking and extending at least substantially to a height of the sidewalls of the single conducting layer and metal layer.

103. (previously presented) The structure of claim 102, wherein the dielectric layer is silicon oxide or BPSG.

104. (previously presented) The structure of claim 102, wherein the metal layer is a first metal layer comprising Ti, Ta, W, Co or Mo or alloys or compounds thereof, including TaN or TiN.

105. (previously presented) The structure of claim 104, further including a second metal layer disposed between the first metal layer and the substrate and comprising TiN, TiW, WN, or TaN.

106. (previously presented) The structure of claim 105, wherein the first metal layer comprises titanium or titanium nitride.

107. (previously presented) The structure of claim 102, wherein the metal layer is titanium or titanium nitride.

108. (previously presented) The structure of claim 102, wherein the single conducting layer is selected from the group comprising aluminum and copper.

109. (previously presented) The structure of claim 108, wherein the single conducting layer is an aluminum-copper alloy.

110. (previously presented) The structure of claim 102, wherein the metal spacers comprise at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN.

111. (previously presented) The structure of claim 102, wherein the metal spacers are titanium or titanium nitride.

112. (previously presented) The structure of claim 102, further comprising a dielectric layer on the single conducting layer and having sidewalls aligned with the sidewalls of the single conducting layer, the metal spacers extending along the sidewalls of the dielectric layer.

113. (previously presented) The structure of claim 112, wherein the dielectric layer comprises a low dielectric constant material.

114. (previously presented) The structure of claim 113, wherein the dielectric layer is fluorine-doped silicon oxide.

115. (previously presented) The structure of claim 102, wherein the metal layer and the metal spacers comprise the same metal.

116. (previously presented) A structure for transmitting a signal laterally across a substrate of a semiconductor device, the structure comprising:

a substrate having a metal layer of a conductive line disposed thereon;

a dielectric layer above the metal layer, the dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer, the aperture at least extending a length of the conductive line;

a metal spacer flanking at least one sidewall of the at least one sidewall of the aperture and in contact with the dielectric layer, the metal spacer in contact with the underlying metal layer; and

a conductive layer in contact with the metal layer and the metal spacer, the metal spacer and the conductive layer substantially filling the aperture, the conductive layer having an upper surface substantially coincident with an upper surface of the dielectric layer.

117. (previously presented) The structure of claim 116, wherein the metal layer comprises tantalum, titanium, tungsten, cobalt, molybdenum, or an alloy or a compound of any thereof, including TaN and TiN.

118. (previously presented) The structure of claim 117, wherein the metal layer is titanium or titanium nitride.

119. (previously presented) The structure of claim 116, wherein the metal spacer includes at least one layer of metal comprising tantalum, titanium, tungsten, cobalt, molybdenum, or alloys or compounds thereof, including TaN and TiN.

120. (previously presented) The structure of claim 119, wherein the metal spacer is titanium or titanium nitride.

121. (previously presented) The structure of claim 116, wherein the substrate comprises a dielectric layer underlying the metal layer.

122. (previously presented) The structure of claim 121, wherein the dielectric layer underlying the metal layer is silicon oxide or BPSG.

123. (previously presented) The structure of claim 116, wherein the metal layer and the metal spacer comprise the same metal.

124. (previously presented) The structure of claim 116, wherein the metal layer is a first metal layer comprising Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

125. (previously presented) The structure of claim 124, further including a second metal layer disposed between the first metal layer and the substrate and comprising TiN, TiW, WN, or TaN.

126. (previously presented) A structure for transmitting a signal laterally across a substrate of a semiconductor device, the structure comprising:

a substrate having a metal layer of a conductive line disposed thereon;

a dielectric layer above the metal layer, the dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer, the aperture at least extending a length of the conductive line;

a metal spacer flanking at least one sidewall of the at least one sidewall of the aperture and in contact with the dielectric layer, the metal spacer in contact with the underlying metal layer;

a conductive layer in contact with the metal layer and the metal spacer, the metal spacer and the conductive layer nearly filling the aperture; and

at least one upper metal layer on the conductive layer and comprising Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN, the at least one upper metal layer being disposed within the aperture laterally adjacent the metal spacer and having an upper surface substantially coincident with an upper surface of the dielectric layer and an uppermost extent of the metal spacer.

127. (previously presented) The structure of claim 126, wherein the at least one upper metal layer comprises a plurality of upper metal layers.

128. (previously presented) The structure of claim 126, wherein the at least one upper metal layer comprises titanium or titanium nitride.

129. (previously presented) The structure of claim 116, wherein the metal spacer extends substantially a height of the at least one sidewall.